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Amendments to the Claims

1. (Previously Presented) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate adjacent to said P well;

an N type active region defined in said P well;

a P type active region defined in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer over said N type active region and a P+ polysilicon layer over said P type active region; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure on a portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, and over only a portion of said isolation region.

2. (Previously Presented) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor, and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure on a portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, and over only a portion of said isolation region.

3. (Previously Presented) A memory cell comprising:

a semiconductor substrate having first and second gate oxide layers;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region, and separate said first and second gate oxide layers;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer on said first gate oxide layer and on a first portion of said isolation region and forming a portion of said NMOS transistor, and a P+ polysilicon layer on said second gate oxide layer and on a second portion of said isolation region and forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only one of said first and second portions of said isolation region, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

4. (Previously Presented) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrat ;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure on said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said oxide diffusion barrier layer does not extend over a portion of said N+ polysilicon layer.

5. (Previously Presented) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure on said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines an N type common boundary with said N+ polysilicon layer that is significantly larger

than a P type common boundary defined by said metal, metal silicide, or metal nitride film and said P+ polysilicon layer.

6. (Previously Presented) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

7. (Previously Presented) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure on a portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said oxide diffusion barrier layer does not extend over a portion of said P+ polysilicon layer.

8. (Previously Presented) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure on a portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines a P type common boundary with said P+ polysilicon layer that is significantly larger than an N type common boundary defined by said metal, metal silicide, or metal nitride film and said N+ polysilicon layer.

9. (Canceled)

10. (Previously Presented) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film on a portion of said polycrystalline silicon film, and over only a portion of said isolation region.

11. (Previously Presented) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film having a thickness of between about 500 Å and about 4000 Å and an overlying metal, metal silicide, or metal nitride film having a thickness of between about 500 Å and 4000 Å, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer having a thickness of between about 3 Å and about 25 Å formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film on a portion of said polycrystalline silicon film, and over only a portion of said isolation region.

12. (Canceled)

13. (Previously Presented) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said polysilicide gate electrode

structure and said oxide diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

14. (Previously Presented) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

15. (Previously Presented) A memory cell array comprising a plurality of SRAM cells arranged in rows and columns, wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film on a portion of said polycrystalline silicon film, and over only a portion of said isolation region.

16. (Previously Presented) A computer system including a microprocessor in communication with a memory cell array via a data communication path, wherein said memory cell array comprises a plurality of SRAM cells arranged in rows and columns, and wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film on a portion of said polycrystalline silicon film and over only a portion of said isolation region.

17- 20. (Canceled)

21. (Previously Presented) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer comprises silicon dioxide.

22. (Previously Presented) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of less than 125 Å.

23. (Previously Presented) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 10 Å and about 15 Å.

24. (Previously Presented) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 3 Å and about 125 Å.

25. (Previously Presented) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 3 Å and about 50 Å.

26. (Previously Presented) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 3 Å and about 125 Å and said polycrystalline silicon film has a thickness of between about 500 Å and about 4000 Å.

27. (Previously Presented) A memory cell as claimed in claim 5 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said P+ polysilicon layer and wherein said oxide diffusion barrier layer is formed in said polysilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said P+ polysilicon layer over the entire extent of said overcoated portion of said P+ polysilicon layer.

28. (Previously Presented) A memory cell as claimed in claim 8 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said N+ polysilicon layer and wherein said oxide diffusion barrier layer is formed in said polysilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said N+ polysilicon layer over the entire extent of said overcoated portion of said N+ polysilicon layer.

29-30. (Canceled)

31. (Previously Presented) A gate electrode structure for a semiconductive device having N type and P type active regions separated by an isolation region, said gate electrode structure comprising:

a film having an N+ polysilicon layer over the N type active region and a P+ polysilicon layer over the P type active region;

an oxide layer formed on a portion of said film and over only a portion of said isolation region; and

a metal, metal silicide, or metal nitride film overlaying said film and said oxide layer.

32. (Canceled)

33. (Previously Presented) A gate electrode structure as claimed by claim 31 wherein said oxide layer is formed on said N+ polysilicon layer.

34. (Previously Presented) A gate electrode structure as claimed by claim 31 wherein said oxide layer is formed on said P+ polysilicon layer.

35. (Canceled)

36. (Previously Presented) A gate electrode structure as claimed by claim 31 wherein said N+ polysilicon layer forms a portion of a pull-down transistor, and said oxide layer is formed on said N+ polysilicon layer.

37. (Previously Presented) A gate electrode structure as claimed by claim 31 wherein said P+ polysilicon layer forms a portion of a pull-up transistor, and said oxide layer is formed on said P+ polysilicon layer.

38. (Previously presented) A gate electrode structure as claimed by claim 31 wherein said oxide layer is silicon dioxide.

39. (Previously presented) A gate electrode structure as claimed by claim 31 wherein said oxide layer has a thickness under 125 Å.

40. (Previously Presented) A memory cell comprising:

a semiconductor substrate having first and second gate oxide layers;

a P well formed in said semiconductor substrate;

a N well formed in said semiconductor substrate adjacent to said P well;

a N type active region defined in said P well;

a P type active region defined in said N well;

an isolation region arranged to isolate said N type active region from said P type active region, and separate said first and second gate oxide layers; and

a gate electrode structure having a film with an N+ polysilicon layer on said first gate oxide layer over said N type active region and on a first portion of said isolation region, and a P+ polysilicon layer on said second gate oxide layer over said P type active region and on a second portion of said isolation region, an oxide layer formed on a portion of said film and

over only one of said first and second portions of said isolation region, and a metal, metal silicide, or metal nitride film overlaying said film and said oxide layer.

41. (New) A gate electrode structure for a semiconductive device having N type and P type active regions separated by an isolation region, said gate electrode structure comprising:

a first layer having an N+ polysilicon portion over the N type active region and a P+ polysilicon portion over the P type active region;

a second layer having a material selected from the group comprising a metal, metal silicide, and metal nitride; and

an oxide layer formed between and in contact with both said first and second layers, wherein said oxide layer is noncoplanar with said first layer and extends over at least a portion of the isolation region.

42. (New) A gate electrode structure as claimed by claim 41 wherein said oxide layer is formed on said N+ polysilicon portion.

43. (New) A gate electrode structure as claimed by claim 41 wherein said oxide layer is formed on said P+ polysilicon portion.

44. (New) A gate electrode structure as claimed by claim 41 wherein said N+ polysilicon portion forms part of a pull-down transistor, and said oxide layer is formed on said N+ polysilicon portion.

45. (New) A gate electrode structure as claimed by claim 41 wherein said P+ polysilicon portion forms part of a pull-up transistor, and said oxide layer is formed on said P+ polysilicon portion.

46. (New) A gate electrode structure as claimed by claim 41 wherein said oxide layer is silicon dioxide.

47. (New) A gate electrode structure as claimed by claim 41 wherein said oxide layer has a thickness under 125 Å.

48. (New) A memory cell comprising:

a semiconductor substrate having first and second gate oxide layers;

a P well formed in said semiconductor substrate;

a N well formed in said semiconductor substrate adjacent to said P well;

a N type active region defined in said P well;

a P type active region defined in said N well;

an isolation region arranged to isolate said N type active region from said P type active region and to separate said first and second gate oxide layers;

a polycrystalline silicon layer overlaying said oxide layers and said isolation region, said polycrystalline silicon layer having an N+ polysilicon portion over said N type active region and a P+ polysilicon portion over said P type active region;

a metal, metal silicide, or metal nitride film layer overlying said polycrystalline silicon layer; and

an oxide layer formed between and in contact with both said polycrystalline silicon layer and said a metal, metal silicide, or metal nitride film layer, wherein said oxide layer is noncoplanar with said polycrystalline silicon layer and extends over at least a portion of said isolation region.